Characterization of PCB Fabrication Processes for a Systematic and Efficient Design of Microstrip Circuits

Owen Casha

***Abstract*— This paper proposes an algorithm to aid in the characterization of a printed circuit board fabrication process before the design of microstrip circuits. By accurately characterizing the electrical properties of a printed circuit board process, one can achieve a systematic and efficient design of microstrip circuits with reduced iteration cycles. The algorithm employs a mean-squared-error optimization technique while making use of de-embedded scattering parameter data from some sample microstrip transmission lines, to estimate printed circuit board electrical parameters such as the tangent loss and the relative permittivity, for a particular frequency range.**

I. INTRODUCTION

Microstrip circuits are essential in modern radio frequency (RF) and microwave engineering, offering low-cost, compact, and high-performance solutions for various applications [1]. Their planar configuration allows easy integration with active and passive components, facilitating the development of advanced and complex communication systems. By employing printed circuit board (PCB) fabrication techniques, microstrip designs ensure compatibility with mass production, minimizing cost and complexity. Their ability to support wide bandwidths and excellent signal integrity makes them ideal for applications ranging from satellite communications to 5G networks [2], [3]. Furthermore, microstrip circuits enable high-density integration in devices such as phased array antennas, filters, amplifiers, and frequency synthesizers [4], [5], [6].

The main challenge in designing microstrip circuits is having access to accurate values of the electrical parameters of the PCB fabrication process to be used, such as the tangent loss ($tan\ \delta$) and the relative permittivity ε_r, particularly for the frequency range of interest [7]. While PCB fabrication firms provide such data, they are often specified at a single frequency which is much lower than that required for a particular application. Using inaccurate values often leads to multiple design iterations and optimization steps before achieving the desired specifications. Thus, this work proposes an algorithm to aid in the characterization of a PCB fabrication process before the design stage of a microstrip circuit. By accurately characterizing the electrical properties of a PCB process one would be able to achieve a systematic and efficient design of microstrip circuits with reduced iteration cycles.

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II. MICROSTRIP CIRCUITS DESIGN TOOL

A. Microstrip Structures: Theory and Background

A microstrip is a planar transmission line used extensively in microwave and millimeter-wave circuits. As shown in Fig. 1, it consists of a thin conducting strip with a width W separated from a ground plane by a dielectric substrate of thickness H, allowing easy integration with PCB technology.

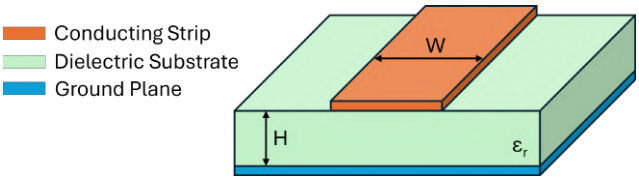

Fig. 1. Generic microstrip structure.

The electromagnetic fields in a microstrip propagate partly in the substrate and partly in the surrounding air, leading to an effective dielectric constant ε_{reff} that is lower than that of the substrate alone (ε_r) [8]:

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + \frac{12}{x}}} \tag{1}$$

where $x = \frac{W}{H}$. The characteristic impedance Z_o depends on the conductor width W, the substrate thickness H, and the dielectric constant ε_r, as per empirical Eq. (2) and Eq. (3) [8].

$$Z_o = \frac{60}{\sqrt{\varepsilon_{reff}}} \ln\left(\frac{8}{x} + \frac{x}{4}\right) \tag{2}$$

when $x \leq 1$ and

$$Z_o = \frac{\frac{120\pi}{\sqrt{\varepsilon_{reff}}}}{x + 1.393 + 6.667 \ln(x + 1.444)} \tag{3}$$

when $x > 1$. Due to relatively high losses at elevated frequencies, careful selection of the substrate material and the conductor thickness is crucial. The losses in a microstrip structure are predominantly affected by the conductor resistivity and the tangent loss of the dielectric material. The tangent loss is defined by Eq. (4) [8]:

$$tan\delta = \frac{-\omega\varepsilon_r'' - \sigma_{sub}}{\omega\varepsilon_r'} \tag{4}$$

where $\varepsilon_r = \varepsilon_r' + j\varepsilon_r''$, σ_{sub} is the conductivity of the dielectric substrate and j is the imaginary unit. The value of σ_{sub} is around 10-11 S/m, so it is typically ignored for commercially available PCB substrates. Microstrip lines support

quasi-transverse electromagnetic mode (TEM) propagation, making their analysis more complex than purely TEM structures. However, robust techniques such as the quasi-static approximation and full-wave electromagnetic solvers are commonly employed for accurate modeling [8]. Ground plane integrity and conductor surface roughness significantly impact performance, particularly at high frequencies.

B. PCB Process Characterization and Modeling

This section describes the PCB process characterization methodology and the algorithm developed to accurately obtain the values of the electrical parameters of some sample test structures including the characteristic impedance Z_o, the tangent loss ($tan\ \delta$) and the relative permittivity ε_r. Initially, a number of microstrip-based transmission line sections of various widths W and fixed length L are fabricated using the chosen PCB process featuring a substrate thickness H (refer to Fig. 2). These will act as the sample test structures.

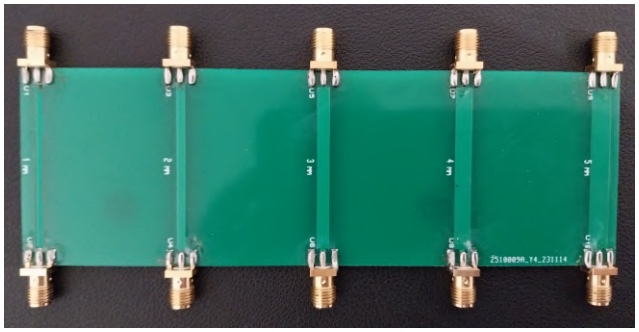

Fig. 2. Fabricated microstrip based transmission line sections of various widths (W = 1 mm to 5 mm) and fixed length (L = 40 mm) on a substrate with thickness H = 1.6 mm.

The scattering parameters (S-parameters) of the fabricated transmission lines are obtained in Touchstone format [8] for a given frequency range using a two-port measurement via a vector network analyzer (VNA), with a given port characteristic impedance (typically 50 Ω). The following algorithm is then applied to each of the sample structures. The measured S-parameters are first de-embedded from the S-parameters of the RF SMA connectors (to be obtained from the manufacturer). Both the measured S-parameters and the connector S-parameters are converted into their respective chain scattering parameters (T-parameters) [8] which are used in Eq. (5) for the de-embedding process:

$$[T_D] = \begin{bmatrix} T_{C11} & T_{C12} \\ T_{C21} & T_{C22} \end{bmatrix}^{-1} \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} T_{C11} & T_{C12} \\ T_{C21} & T_{C22} \end{bmatrix}^{-1} \quad (5)$$

where $[T_D]$ are the de-embedded T-parameters of the sample structures, $[T_C]$ are the T-parameters of the RF SMA connectors and $[T]$ are the T-parameters of the sample structures including the RF connectors. Following this process, $[T_D]$ is then converted back to S-parameters $[S_a]$. The algorithm must be provided with some fixed parameters: the width W and the length L of the microstrip structure, the dielectric substrate thickness H, the characteristic impedance of the VNA, the initial values of the three transmission line parameters to be determined (Z_o, ε_{reff} and $\tan\delta$) together with the number of iterations n_{max} to be considered in the model fitting and the number of data points p for each parameter sweep. For each iteration n, a set of p values for Z_o, ε_{reff} and $\tan\delta$ are generated using Eq. (6)-(8):

$$(1-v)Z_o[n-1] \le Z_o[n,p] \le (1+v)Z_o[n-1] \quad (6)$$

$$(1-v)\varepsilon_{reff}[n-1] \le \varepsilon_{reff}[n,p] \le (1+v)\varepsilon_{reff}[n-1] \quad (7)$$

$$(1-v)\tan\delta[n-1] \le \tan\delta[n,p] \le (1+v)\tan\delta[n-1] \quad (8)$$

where $Z_o[n,p]$, $\varepsilon_{reff}[n,p]$ and $\tan\delta[n,p]$ are the p transmission line model values for the current iteration index n, v is the fractional variation from the nominal values $Z_o[n-1]$, $\varepsilon_{reff}[n-1]$ and $\tan\delta[n-1]$, which are the model values chosen from the previous iteration. In this algorithm, v is reduced on each iteration according to Eq. (9):

$$v = r^n \quad (9)$$

to avoid over-fitting of the three transmission line parameters, where r is a fractional empirical constant that is set by the user. The higher the value of r, the larger the parameter sweeping range for each iteration. During every iteration n, for each value of Z_o, ε_{reff} and $\tan\delta$, an ABCD frequency-dependent matrix representation of the microstrip transmission line section is generated using Eq. (10) [8], for the number of frequency points f_n available in the Touchstone format de-embedded S-parameters dataset.

$$\begin{bmatrix} A(f) & B(f) \\ C(f) & D(f) \end{bmatrix} = \begin{bmatrix} \cosh\gamma L & Z_o \sinh\gamma L \\ \frac{\sinh\gamma L}{Z_o} & \cosh\gamma L \end{bmatrix} \quad (10)$$

where γ is the propagation coefficient given by Eq. (11):

$$\gamma = \alpha + j\beta \quad (11)$$

The attenuation coefficient α is given by Eq. (12):

$$\alpha = \frac{2\pi f}{c}\sqrt{\frac{\varepsilon_{reff}}{2}}\left(\sqrt{1+(\tan\delta)^2}-1\right) \quad (12)$$

and the phase coefficient β is determined by Eq. (13):

$$\beta = \frac{2\pi}{\lambda} = \frac{2\pi f\sqrt{\varepsilon_{reff}}}{c} \quad (13)$$

where c is the velocity of propagation in free space and f is the frequency. Eq. (12) models the PCB substrate losses. All the generated model ABCD matrices are converted into S-parameter matrices $[S_m]$ [8] and are then compared to the measured de-embedded S-parameters $[S_a]$ of the sample microstrip structure to identify which set of transmission line parameters (Z_o, ε_{reff} and $\tan\delta$) gives the minimum mean-square-error or cost function η using Eq. (14):

$$\eta = \frac{\sum\Big(|S_{11a}(f)| - |S_{11m}(f,\tan\delta,Z_o,\varepsilon_{reff})|\Big)^2}{f_n} + \frac{\sum\Big(|S_{21a}(f)| - |S_{21m}(f,\tan\delta,Z_o,\varepsilon_{reff})|\Big)^2}{f_n} \quad (14)$$

where f_n is the number of frequency points, $S_{11a}(f)$ is the measured reflection coefficient at port 1 and $S_{21a}(f)$ is the measured transmission coefficient over the considered frequency range, and $S_{11m}(f)$ is the modeled reflection coefficient at port 1 and $S_{21m}(f)$ is the modeled transmission coefficient over the considered frequency range. Once the values of Z_o, ε_{reff} and $\tan\delta$ are determined, they are stored and used as the initial values for the next iteration, unless the maximum number of iterations set by the user has been reached. The cost function η is used to quantify the discrepancy between the measured data and the modeled data for S_{11} and S_{21}. By minimizing η, the parameters that optimally match the modeled and measured S-parameters of the microstrip structures are found. The cost function sums up all these squared differences (for each frequency point) and then divides by the number of frequency points f_n. This effectively takes the mean-squared error for each scattering parameter over the frequency band of interest. This PCB process characterization and modeling algorithm is summarised in Fig. 3.

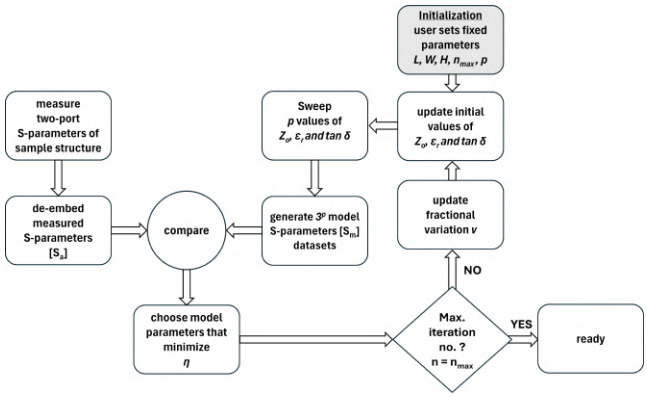

Fig. 3. Principle of the proposed printed circuit board (PCB) process characterization and modeling algorithm.

C. PCB Process Test Case

This section presents the characterization results of the five different sample microstrip structures shown in Fig. 2. These were fabricated using a high-performance FR-4 double-sided PCB process with a high glass transition temperature, and low coefficient of temperature expansion substrate featuring a nominal relative permittivity of 4.6 and a thickness H of 1.6 mm. Table I presents the estimated values of Z_o, ε_{reff}, ε_r and $\tan\delta$ for the five sample microstrip structures. Table I also presents the final cost function value η for each microstrip structure sample, indicating a good fit is achieved in each case. The data presented in Table I was obtained using the proposed algorithm with $n_{max} = 40$, $p = 10$, and $r = 0.85$.

TABLE I
PARAMETER ESTIMATION OF THE MICROSTRIP STRUCTURE SAMPLES

Parameter	1 mm	2 mm	3 mm	4 mm	5 mm
$\tan\delta$	0.0118	0.0117	0.0119	0.012	0.0122
$Z_o(\Omega)$	85.97	62.21	49.43	41.23	35.44
ε_{reff}	3.221	3.368	3.452	3.574	3.654
ε_r	4.634	4.623	4.586	4.638	4.649
η (10^{-3})	0.8966	0.6162	0.8620	1.3357	1.935

As an example, Fig. 4 shows the variation of the cost function η and the estimated parameters (Z_o, ε_{reff}, ε_r and $\tan\delta$) with the iteration number for the fabricated 1 mm microstrip transmission line structure.

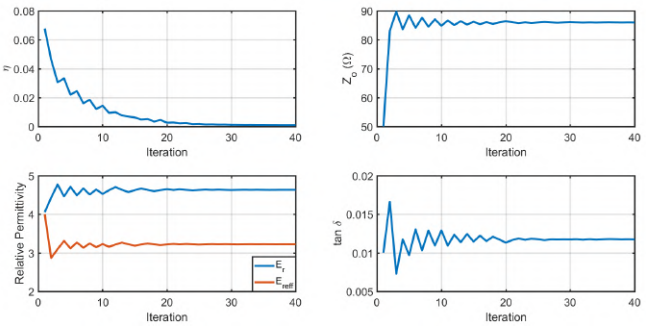

Fig. 4. Estimated parameters and cost function value η for the 1 mm microstrip transmission line structure .

Fig. 5 presents the frequency response of both the measured and the modeled return loss and insertion loss of the fabricated microstrip transmission line structure. The results confirm that the algorithm achieves a good fit and that the parameters are estimated with adequate accuracy to aid the design of microstrip circuits.

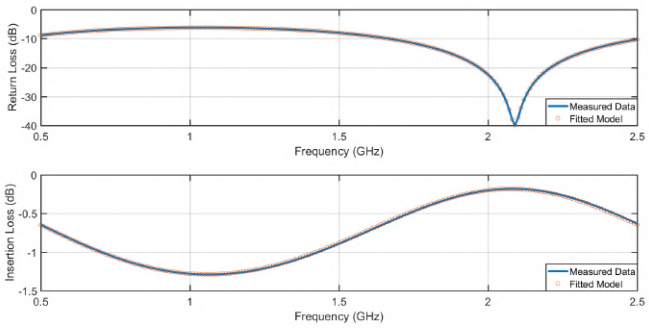

Fig. 5. Frequency response of the measured and the modeled return loss and insertion loss of the fabricated microstrip transmission line structure.

Using the estimated values for Z_o and ε_{reff}, it is possible to obtain a polynomial fitting for these parameters to model their variation with the microstrip width W (refer to Fig. 6). These polynomials are used to design the actual microstrip circuits, as discussed in Section III.

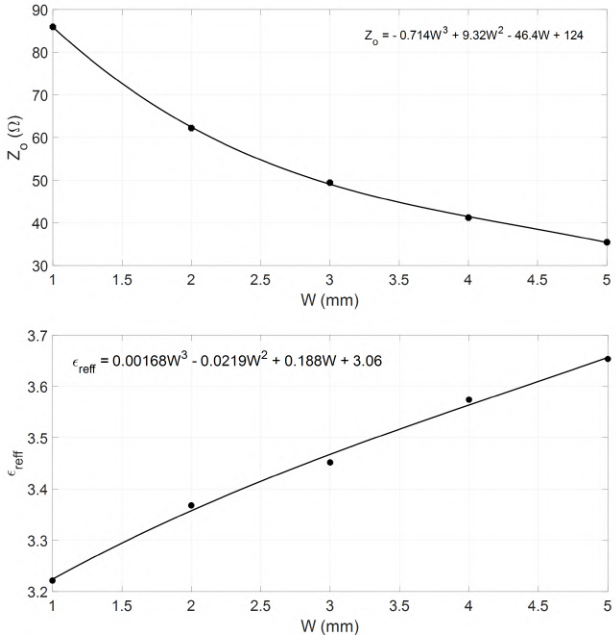

Fig. 6. 3^{rd} order polynomial fitting for Z_o and ε_{reff}.

III. MICROSTRIP CIRCUIT DESIGNS

This section presents the design and characterization of some microstrip circuits, including two impedance transformers and a Wilkinson power divider. These circuits are based on different microstrip structures of a certain length and characteristic impedance Z_o. An FR-4 double-sided PCB process featuring a nominal relative permittivity of 4.6 and a thickness H of 1.6 mm was used. The polynomials presented in Fig. 6, which were estimated using the algorithm proposed in Section II, were used to efficiently design these circuits by accurately calculating the width W required to achieve the characteristic impedance Z_o and effective relative permittivity ε_{reff} of certain microstrip structures (refer to Table II). For each structure, the wavelength is also calculated using Eq. (13). The S-parameter measurements were carried out using the Siglent SVA 1032X vector network analyzer.

TABLE II
DESIGN PARAMETERS OF THE MICROSTRIP STRUCTURES

$Z_o(\Omega)$	W (mm)	$\lambda(mm)$	ε_{reff}
50	2.94	161.14	3.46612
70.7	1.60	164.80	3.31162
75	1.41	165.43	3.28625

A. $\lambda/4$ *Impedance Transformer*

A quarter-wavelength transformer is an impedance-matching network consisting of a transmission line section with a length equal to an odd multiple of one-quarter of the signal's wavelength [8]. It is used to match a load impedance to a source impedance by selecting the characteristic impedance of the transformer as the geometric mean of the two impedances, thereby minimizing signal reflections. In this work, a 100 Ω to 50 Ω 1 GHz impedance transformer was designed and fabricated using a microstrip structure with a characteristic impedance of $\sqrt{100\times 50} = 70.7$ Ω and a length of 164.80/4 = 41.2 mm. The PCB layout is shown in Fig. 7.

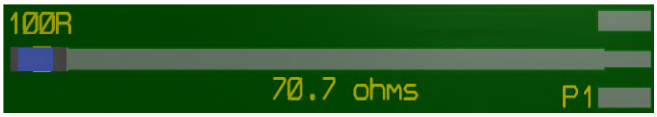

Fig. 7. PCB layout of the narrowband 1 GHz quarter-wavelength impedance transformer.

The measured frequency response of the impedance transformer is shown in Fig. 8 and was obtained via a one-port VNA measurement using SMA RF connectors, where the return loss at port P_1 and the input impedance Z_{11} are presented. A return loss of around -38.6 dB and $Z_{11} = 48.9 + j0.215$ Ω were achieved at a resonant frequency of 1 GHz as required.

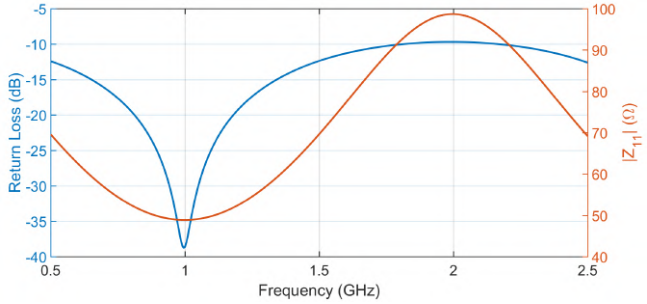

Fig. 8. Measured performance of the narrowband 1 GHz quarter wavelength 100 Ω to 50 Ω impedance transformer.

B. $\lambda/12$ *Impedance Transformer*

Fig. 9 shows the PCB layout of a one-twelfth impedance transformer, designed to convert an impedance of 75 Ω to 50 Ω at 1 GHz. The twelfth-wave transformer is an alternative to the more well-known quarter-wavelength transformer presented in Section IIIA [9].

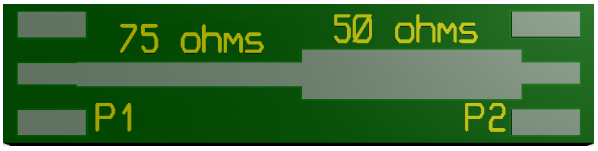

Fig. 9. PCB layout of the $\lambda/12$ impedance transformer.

With the twelfth-wave transformer, two lengths of microstrip structures are used in series, each having an electrical length of nearly one twelfth-wavelength, but of characteristic impedances equal to the two impedances Z_{o1} and Z_{o2} being matched. The actual length d of each microstrip structure is given by Eq. (15) [9]:

$$d = \frac{\lambda \arctan\left(\sqrt{\frac{B}{B^2+B+1}}\right)}{2\pi} \tag{15}$$

where $B = \frac{Z_{o1}}{Z_{o2}}$. For $Z_{o1} = 75\ \Omega$ and $Z_{o2} = 50\ \Omega$, the length d is equal to 0.08148λ or 13.48 mm for the 75 Ω transmission line section and 13.13 mm for the 50 Ω transmission line section, using the information provided in Table II. The measured frequency response of the $\lambda/12$ impedance transformer is shown in Fig. 10 and was obtained via a one-port VNA measurement while port P_2 was terminated with a 75 Ω dummy load connected via an RF SMA connector. A return loss of around -49 dB and a $Z_{11} = 49.7 - j0.04\ \Omega$ were achieved at a resonant frequency of 1 GHz.

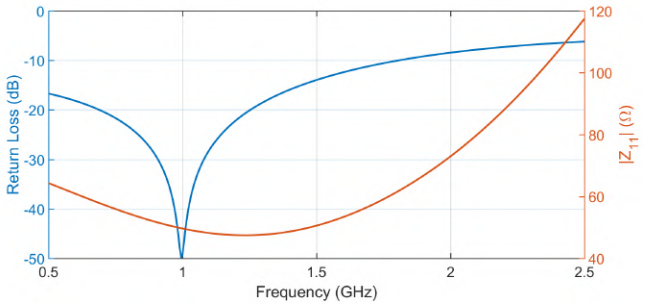

Fig. 10. Measured performance of the $\lambda/12$ impedance transformer.

C. Wilkinson Power Divider

Fig. 11 shows the design of a 1 GHz microstrip Wilkinson power divider, which is a passive microwave network that evenly splits an input signal (fed into port P_1) into two output signals with equal amplitude and phase while maintaining impedance matching at all ports [8]. It uses quarter-wave transmission line transformers with a characteristic impedance of 70.7 Ω and length of 41.2 mm, together with a thin film surface mount isolation resistor of 100 Ω, to ensure minimal reflection and high isolation between output ports (P_2 and P_3).

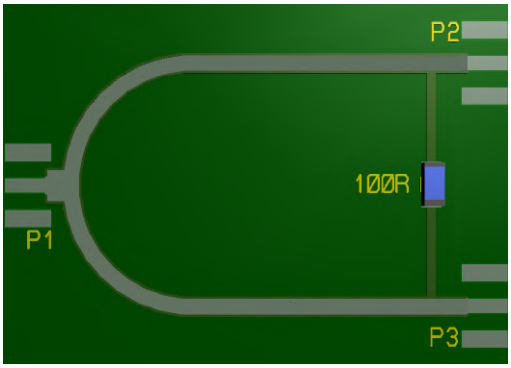

Fig. 11. PCB layout of the narrowband Wilkinson power divider.

The measured frequency response of the power divider is shown in Fig. 12. A return loss of -36 dB was achieved at port P_1 while a return loss of -38 dB was achieved at ports P_2 and P_3. The design features an isolation of more than -50 dB between ports P_2 and P_3 and an insertion loss of -3.11 dB at 1 GHz. The insertion loss is lower than the expected value of -3 dB due to the finite tangent loss of the PCB fabrication process.

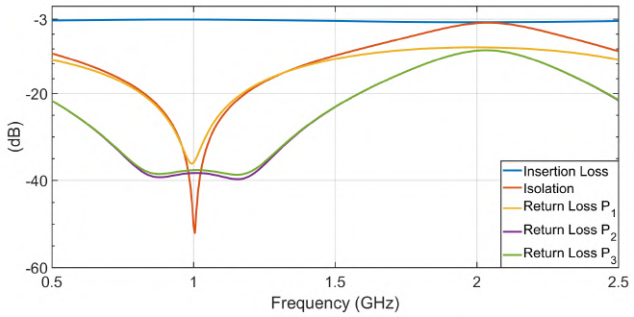

Fig. 12. Measured performance of the narrowband 1 GHz Wilkinson power divider.

IV. CONCLUSION

This paper presented an algorithm to aid in the characterization of a PCB fabrication process before the design of microstrip circuits. By accurately obtaining the values of the electrical properties of a PCB process, including the tangent loss and the relative permittivity of the substrate for a particular frequency range, one can achieve a systematic and efficient design of microstrip circuits with reduced iteration cycles. The algorithm employs a mean-squared-error optimization technique while making use of de-embedded scattering parameter data from some pre-fabricated sample microstrip transmission lines. This paper showed the algorithm's effectiveness through some microstrip circuit designs, including two impedance transformers and a Wilkinson power divider.

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